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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SURESH MARISETTY,
GEORGE THANGADURAI, and MANI AYYAR

Appeal 2007-4338
Application 10/628,726
Technology Center 2100

Decided: August 19, 2008

Before KENNETH W. HAIRSTON, ALLEN R. MACDONALD,
and LINDA E. HORNER, *Administrative Patent Judges*.

HAIRSTON, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants seek our review under 35 U.S.C. § 134 of the Examiner's final rejection of claims 5-19 and 24-26. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part.

INVENTION

Appellants' claimed invention is directed to a processor included in a multiple processor system which detects an error and initiates a rendezvous state during which all other processors become idle to allow the processor to correct the error and, thereafter, return the system back to normal operation (Spec. 13-14 and Fig. 4 & 5).

Claim 5, reproduced below, is representative of the subject matter on appeal:

5. A system, comprising:

a non volatile memory to store an error handling routine and an idle routine, said error handling routine to permit a computer system to continue operating when an error is detected;

a plurality of slave processors to execute the idle routine, wherein the plurality of slave processors are included in the computer system; and

a monarch processor included in the computer system, the monarch processor being capable of executing the error handling routine to correct the error.

THE REJECTIONS

The Examiner relies upon the following as evidence of unpatentability:

Fujii	US 5,892,898	Apr. 06, 1999
Falik	US 6,065,078	May 16, 2000
Bowers	US 6,308,285 B1	Oct. 23, 2001

The following rejections are before us for review:

1. Claims 24-26 stand rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter.

2. Claims 5-16 and 24-26 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Bowers.

3. Claims 18 and 19 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Falik.

4. Claim 17 stands rejected under 35 U.S.C. § 103(a) as being obvious over Bowers in view of Fujii.

NON-STATUTORY SUBJECT MATTER REJECTION UNDER § 101

Initially, we note that claims 24-26 were argued as a group with claim 24 as representative (App. Br. 13). Thus, claims 25-26 stand or fall with claim 24.

The issue before us is whether the Examiner erred in rejecting claims 24-26 under 35 U.S.C. § 101 as being directed to non-statutory subject matter. The issue turns on whether "[a]n article comprising a machine-accessible medium having associated data, wherein the data, when accessed, results in a machine performing" a set of functions as recited in claim 24, constitutes an article of manufacture.

PRINCIPLES OF LAW

The scope of patent-eligible subject matter includes one of the four enumerated categories of "process, machine, manufacture, or composition of matter." 35 U.S.C. § 101.

> When nonfunctional descriptive material is recorded on some computer-readable medium, in a computer or on an electromagnetic carrier signal, it is not statutory since no requisite functionality is present to satisfy the practical application requirement. Merely claiming nonfunctional descriptive material, i.e., abstract ideas, stored in a computer-readable medium, in a computer, on an electromagnetic carrier signal does not make it statutory. . . . Such a result would exalt form over substance.
>
> MPEP § 2106.01
>
> "[L]ogic" . . . does not require a computer program that implements functions on a computer system or a data structure that modifies a function of the computer system. Rather, the "logic" may be merely textual instructions that do not impart any functionality to a computer system, i.e., the "logic" is merely non-functional descriptive material. *Ex parte ALAN R. SHEALY*, 2007 WL 1196758, Appeal No. 2006-1601 (BPAI).

ANALYSIS

Did the Examiner err in determining that claims 24-26 are directed to non-statutory subject matter?

Appellants argue that:

> In view of the Court's ruling in *Alappat* and *AT&T*, it is respectfully noted that claims 24-26 recite the structure of '[a]n article comprising a machine-accessible medium having associated data, wherein the data, when accessed, results in a machine performing . . .' . These claims are therefore directed to an article of manufacture, including a

> system 500 executing code stored in a system memory 540 (see page 14 of the Application, lines 15-16), and as such, clearly fall into one of the four acceptable statutory categories of patentable subject matter.
> (App. Br. 13).

The Appellants further argue that the claimed article of manufacture is clearly a practical application that achieves a useful, concrete, and tangible final result (Reply Br. 2). Appellants cite *State Street* for the proposition that the focus should not be on which of the four categories of subject matter a claim is directed to, but rather on its practical utility (Reply Br. 2).

The Examiner responds that "a machine-accessible medium can be a piece of paper being scanned. Further, it is unclear as to whether the data is instructions or code and whether it is even stored on a medium" (Ans. 15).

We agree with the Examiner's analysis. We add the following primarily for emphasis.

Claim 24 recites "[a]n article comprising a machine-accessible medium having associated data, wherein the data, when accessed, results in a machine performing" which is then followed by a set of instructions. The conditional language of "when accessed, results in a machine performing" clearly negates any positive recitation of tangible structure, resulting in merely claiming only "a machine-accessible medium having associated data." The Examiner reasonably construed this language as nothing more than a piece of paper with data (Ans. 15). Such a drafting approach of reciting "[a]n article comprising a machine-accessible medium" amounts to no more than a gratuitous recitation of elements for the

purpose of attempting to circumvent a non-statutory subject matter rejection by exalting form over substance.

Furthermore, the "associated data" do not require a computer program that implements functions on a computer system or a data structure that modifies a function of the computer system. *Ex parte ALAN R. SHEALY*, 2007 WL 1196758, Appeal No. 2006-1601 (BPAI). Thus, the "associated data" may be merely textual instructions that do not impart any functionality to a computer system, i.e., the "associated data" is merely non-functional descriptive material. *Id.*

Furthermore, the Examiner is correct in determining that "a machine-accessible medium" is not the same as a "computer-readable medium," and that such broad language could be construed as nothing more than a piece of paper with associated data (Ans. 15), unattached from any storing medium. However, even if the "associated data" were recorded on some computer-readable medium, in a computer, the claim is still not statutory since no requisite functionality is present to satisfy the practical application requirement. MPEP § 2106.01. In other words, merely claiming nonfunctional descriptive material, i.e., data, stored in a computer-readable medium, in a computer does not make it statutory, because such a result would exalt form over substance. *Id.*

For the above reasons, Appellants' arguments have not persuaded us of error in the Examiner's rejection of claims 24-26 under 35 U.S.C. § 101 as being non-statutory, and we sustain the Examiner's rejection.

ANTICIPATION

There are three anticipation issues before us. The first issue is whether Appellants have shown that the Examiner erred in rejecting claims 5-6, 8-16, and 24-26 under 35 U.S.C. § 102(b) as anticipated by Bowers. The first issue specifically turns on whether the Examiner erred in determining that Bowers' controller can be characterized as a "monarch processor." The second issue is whether Appellants have shown that the Examiner erred in rejecting claim 7 under 35 U.S.C. § 102(b) as anticipated by Bowers. The second issue seeks a resolution of the question whether the Examiner erred in determining that Bowers discloses that "the monarch processor is capable of sending a wake up signal to the plurality of slave processors to exit the rendezvous state." The third issue is whether Appellants have shown that the Examiner erred in rejecting claims 18 and 19 under 35 U.S.C. § 102(e) as anticipated by Falik. The third issue turns on whether the Examiner erred in determining that Falik discloses that the rendezvous state is a state "where all but one of the processors included in the multiple processor system are idle" as claimed.

FINDINGS OF FACT

The relevant facts include the following:

1. Appellants' disclosure describes a special definition of the "monarch processor" which includes a processor that is pre-designated and, thus, unable to be placed in rendezvous state since the monarch processor will execute the error handling routine (Spec. 8:22-23 and Spec. 8:24-28).

2. Falik teaches a host computer having a number of debugger processors (i.e., Fig. 18, elements 1830a-1830c and col. 2, ll. 37-43) for each of the monitor processors (i.e., Fig. 18, elements 1840a-1840c and col. 2, ll. 37-43).
3. Falik further teaches that an interrupt message (i.e., entering the rendezvous state) may be sent to a processor (i.e., 1840a to 1840c and col. 4, ll. 30-34) or to multiple processors (i.e., 1840a to 1840c and col. 7, ll. 26-30).

PRINCIPLES OF LAW

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. Inc., v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987).

The claim terms should be given their broadest reasonable meaning in their ordinary usage as such claim terms would be understood by one skilled in the art by way of definitions and the written description. *In re Morris*, 127 F.3d 1048, 1054 (Fed. Cir. 1997).

> The claims, of course, do not stand alone. Rather, they are part of a 'fully integrated written instrument' . . . consisting principally of a specification that concludes with the claims. For that reason, claims 'must be read in view of the specification, of which they are a part.' . . . . [T]he specification 'is always highly relevant to the claim construction analysis. Usually, it is dispositive; it is the single best guide to the meaning of a disputed term.'

Phillips v. AWH Corp., 415 F.3d 1303, 1315 (Fed. Cir. 2005).

The specification may reveal a special definition given to a claim term by the patentee that differs from the meaning it would otherwise possess. In such

cases, the inventor's lexicography governs. *Sinorgchem Co., Shandong v. International Trade Commission*, 511 F.3d 1132, 1136 (Fed. Cir. 2007).

ANALYSIS

Initially, we note that Appellants' arguments have grouped claims 5-6, 8-16, and 24-26 together (App. Br. 14). Thus, in accordance with 37 C.F.R. §41.37(c)(1)(vii) we select claim 5 as representative of the group of claims. Furthermore, we note that Appellants' mere recitation of the claim limitations set forth in the claims on appeal (e.g., claims 8-17 and 24-26) (App. Br. 14-15) is not considered an argument for patentability. Simply pointing out what a claim requires with no attempt to point out how the claim patentably distinguishes over the prior art does not amount to a separate argument for patentability. *In re Nielson*, 816 F.2d 1567, 1572 (Fed. Cir. 1987). Accordingly, as indicated *infra*, claims 6, 8-16 and 24-26, which are subject to the same ground of rejection, fall with claim 5. 37 C.F.R. § 41.37 (c)(1)(vii) (2007). Claim 7 was argued separately, and is addressed *infra*.

Claims 5-6, 8-16, and 24-26

Did the Examiner err in determining that Bowers' controller can be characterized as a "monarch processor?"

Appellants argue that:

> First, . . . Bowers makes a clear distinction between the "controller" and the "processors." It is *only* the controller in Bowers, and not the processors, that can access data used to put the processors to sleep. Second, even if one accepts the premise that Bowers' controller can

> operate as a monarch processor, the conclusion would be that Bowers' controller, as one of the plurality of processors, could also be put to sleep for replacement as directed by one of the other processors in Bowers' system. This type of operation, claimed by the Appellant[s], is not possible using Bowers' system.
> (App. Br. 14).

The Appellants further argue that the Examiner's interpretation of what constitutes a "monarch" processor contradicts the meaning of the term as understood by those skilled in the art (Reply Br. 3). Specifically, Appellants present as a customary meaning that "[i]f the monarch fails, the serfs can usurp its power (deconfigure the monarch) and force a system to reboot, whereupon the arbitration process is repeated and a new monarch selected" (Reply Br. 3).

The Examiner responds that "[i]n column 4, lines 41-67 continued in column 5, lines 1-9, Bowers discloses an operating system of computer 30 that sends signals to controller 112 to place the processors in a sleep state. The combination of an operating system with instructions and a controller that executes the instructions constitute a processor" (Ans. 15). Furthermore, the Examiner states:

> the Appellant[s] never claims that the monarch processor could be any of the plurality of processors. Instead, it appears that there is always one processor pre-selected to be the monarch processor, and that the monarch processor is not capable of being any other processor. For this reason, it is not necessary for the controller of Bowers to be able to be put to sleep.
> (Ans. 16).

We agree with the Examiner's findings of fact and conclusions and adopt them as our own. We add the following primarily for emphasis.

Appellants' disclosure states that "the monarch processor could pre-designated [sic] by design or on system startup" (Finding of Fact 1). Claim 5 does not preclude pre-designation of the monarch processor. Thus, Appellants' disclosure describes a special definition of the "monarch processor" which includes a processor that is pre-designated and, thus, unable to be placed in rendezvous state since the monarch processor will execute the error handling routine (Finding of Fact 1). The Appellants' offered customary meaning of the monarch processor, under which the rest of the processors could overtake the failing monarch and select a new one (Reply Br. 3), runs contrary to Appellants' lexicography of a pre-designated monarch (Spec. 8:22-23). As stated *supra*, in such cases, the inventor's lexicography governs. *Sinorgchem Co., Shandong v. International Trade Commission*, 511 F.3d 1132, 1136 (Fed. Cir. 2007).

Thus, Appellants' argument has not persuaded us of error in the Examiner's rejection since Appellants' disclosed lexicography of a pre-designated monarch governs.

Claim 7

Did the Examiner err in determining that Bowers discloses that "the monarch processor is capable of sending a wake up signal to the plurality of slave processors to exit the rendezvous state" as claimed?

Appellants argue that Bowers fails to disclose that "the monarch processor is capable of sending a wake up signal to the plurality of slave processors to exit the rendezvous state" (App. Br. 15).

The Examiner responds:

> In column 5, lines 2-3, Bowers discloses a controller (monarch processor included in the computer system) that generates a stop clock signal STPCLK# and a sleep signal SLP# (error handling routine to correct an error). And in column 7, lines 4-6, Bowers discloses that when all removals or replacements have been made, the controller will begin the reinitialization sequence to return the computer to normal operation (wherein the monarch processor is capable of sending a wake up signal to the plurality of slave processors to exit the rendezvous state).
> (Ans. 16).

We agree with the Examiner's findings of fact and conclusions and adopt them as our own.

Thus, Appellants' argument has not persuaded us of error in the Examiner's rejection because the controller/monarch sends a signal for reinitializing and returning the computer to normal operation (Ans. 16) and, in other words, the controller/monarch wakes up the slave processors which exit the rendezvous state (i.e., return to normal operation) as claimed.

For the above reasons, Appellants' argument has not persuaded us of error in the Examiner's rejection of claim 7 under 35 U.S.C. § 102(b) as being anticipated by Bowers, and we sustain the Examiner's rejection.

Claims 18 and 19

Did the Examiner err in determining that Falik discloses that the rendezvous state is a state "where all but one of the processors included in the multiple processor system are idle" as claimed?

Initially, we note that Appellants' arguments have grouped claims 18 and 19 together (App. Br. 15-16). Thus, in accordance with 37 C.F.R. § 41.37(c)(1)(vii) we select claim 18 as representative of the group of claims.

Appellants argue:

> [f]inally, how can "all but one of the processors included in the multiple processor system" be idle, as asserted in the Office Action, if at least one processor in Falik's multiprocessor integrated circuit 1810 must be awake to execute a monitor, *in addition* to the processor running the debugger on the host computer? The debugger communicates with the monitor on one of the processors, which means at least *two* processors must be operational to debug programs in Falik's system. See Falik, Col. 17, lines 27-46. This is not what is claimed by the Appellant[s]. (Emphasis in original).
> (App. Br. 16).

The Examiner responds:

> It is clear that all of the monitors on the processors are brought back up and synchronized after the error is corrected. Further, in column 7, lines 26-30, Falik et al. disclose that the interrupt control module issues an ISE interrupt request to either a specific one of the processors or to multiple processors (on failure, entering a rendezvous state to correct the error, said rendezvous state being a state where all but one of the processors included in the multiple processor system are idle).
> (Ans. 20).

Falik teaches a host computer having a number of debugger processors (i.e., 1830a-1830c) for each of the monitor processors (i.e., 1840a-1840c) (Finding of Fact 2). Falik further teaches that an interrupt message (i.e., entering the rendezvous state) may be sent to a single processor or multiple processors (i.e., 1840a to 1840c) (Finding of Fact 3). Thus, if a debugger processor serves as the monarch (i.e., processor 1830a) which places all the monitor processors (i.e., 1840a to 1840c) into an idle state, this still does not meet the limitation of "all but one," because debugger processors 1830b and 1830c would still not be in idle mode.

Thus, we are persuaded by Appellants' argument because Falik does not disclose a "rendezvous state being a state where all but one of the processors included in the multiple processor system are idle" as recited in claim 18.

For the above reasons, Appellants' arguments has persuaded us of error in the Examiner's rejection of claims 18 and 19 under 35 U.S.C. § 102(e) as being anticipated by Falik, and we reverse the Examiner's rejection.

OBVIOUSNESS

There is a single obviousness issue before us regarding whether Appellants have shown that the Examiner erred in rejecting claim 17 under 35 U.S.C. § 103(a).

PRINCIPLES OF LAW

"Section 103 forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such that the subject

matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'" *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1734 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, (3) the level of skill in the art, and (4) where in evidence, so-called secondary considerations. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966). *See also KSR*, 127 S. Ct. at 1734 ("While the sequence of these questions might be reordered in any particular case, the [*Graham*] factors continue to define the inquiry that controls.")

The Examiner bears the initial burden of presenting a prima facie case of obviousness. *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992). If that burden is met, then the burden shifts to the Appellant to overcome the prima facie case with argument and/or evidence. *Id. In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006).

The Supreme Court, quoting *In re Kahn*, 441 F.3d at 988, stated that "rejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness." *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. at 1741. However, "the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *Id.*

ANALYSIS

Appellants argue that there is lack of motivation to combine the Bowers and Fujii references as the word "error" does not appear in Bowers (App. Br. 17). Appellants further argue that the Office mischaracterizes the term "severe error" as "non-recoverable problem" rather than "recoverable error" (App. Br. 17). Finally, Appellants argue that there is "no reasonable expectation of success" (App. Br. 18).

The Examiner responds that "[c]laim 17 fails to mention that the error is recoverable or non-recoverable, but rather, refers to the error as being severe. A nonrecoverable error is severe. For this reason it is reasonable for the Examiner to interpret it as such" (Ans. 21-22). The Examiner further explains that: "The primary reference of Bowers is concerned with replacing processors and only that. Therefore, any error detected in Bowers is concerned with just the processors. Bowers is silent as to how it is determined if the processor should be replaced. Fujii cures this deficiency by relating the severity of errors with appropriate actions" (Ans. 22).

Furthermore, the Examiner articulated the following as a motivation to combine the teachings of the references. "In this case, an error event type is used to report a non-recoverable problem (see Fujii et al.: co1.2, lines 62-63) and a warning event type is used to indicate some kind of recoverable anomaly (see Fujii et al.: col. 2, lines 60-62). Knowing the severity determines what action should be taken (removal of a processor) (see Fujii et al.: col. 2, lines 48-55)" (Ans. 21).

Thus, as stated *supra*, the Examiner's articulated reasoning provides a rational underpinning to support the legal conclusion of obviousness (i.e.,

determination of error severity guides corrective action). *KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. at 1741.

For the above reasons, Appellants' arguments have not persuaded us of error in the Examiner's rejection of claim 17 under 35 U.S.C. § 103(a) as being unpatentable over Bowers in view of Falik, and we sustain the Examiner's rejection.

CONCLUSIONS OF LAW

We conclude that the Appellants have not shown that the Examiner erred in rejecting claims 24-26 as being directed to non-statutory subject matter under 35 U.S.C. § 101. Appellants have not shown that the Examiner erred in rejecting claims 5-16 and 24-26 as anticipated by Bowers under 35 U.S.C. § 102(b). Appellants have shown that the Examiner erred in rejecting claims 18 and 19 as anticipated by Falik under 35 U.S.C. § 102(e). Appellants have not shown that the Examiner erred in rejecting claim 17 as obvious over Bowers in view of Fujii under 35 U.S.C. § 103(a).

DECISION

The decision of the Examiner to reject claims 5-17 and 24-26 is affirmed. The decision of the Examiner to reject claims 18 and 19 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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